FIG. 1

SYSTEM STRUCTURE FOR REALIZING CONTROL METHOD DIRECTED TO FIRST EMBODIMENT

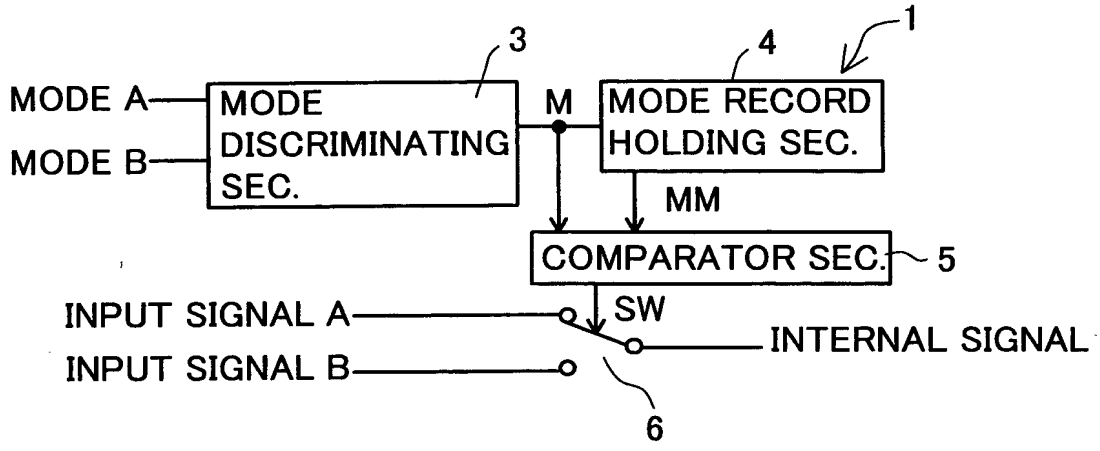

FIG. 2

OPERATIONAL WAVEFORMS OF SYSTEM STRUCTURE DIRECTED TO FIRST EMBODIMENT

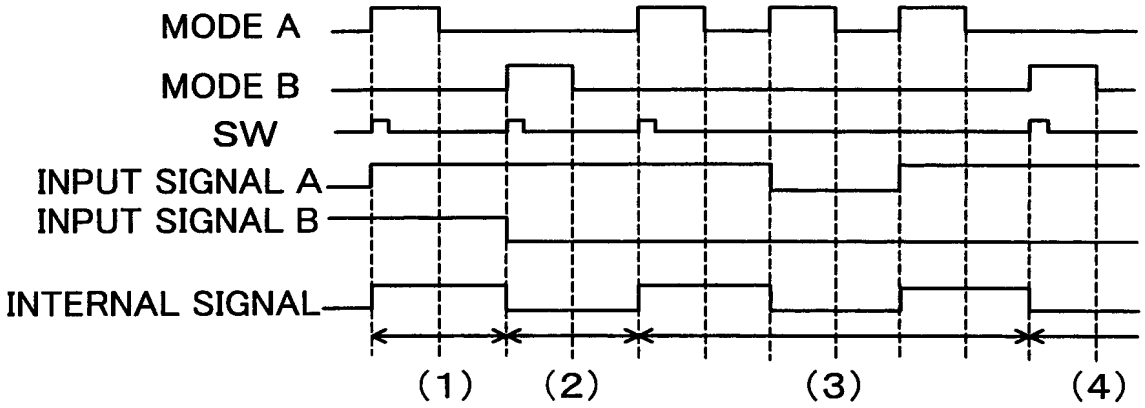

FIG. 3

FLOW CHART SHOWING CONTROL METHOD DIRECTED TO FIRST EMBODIMENT

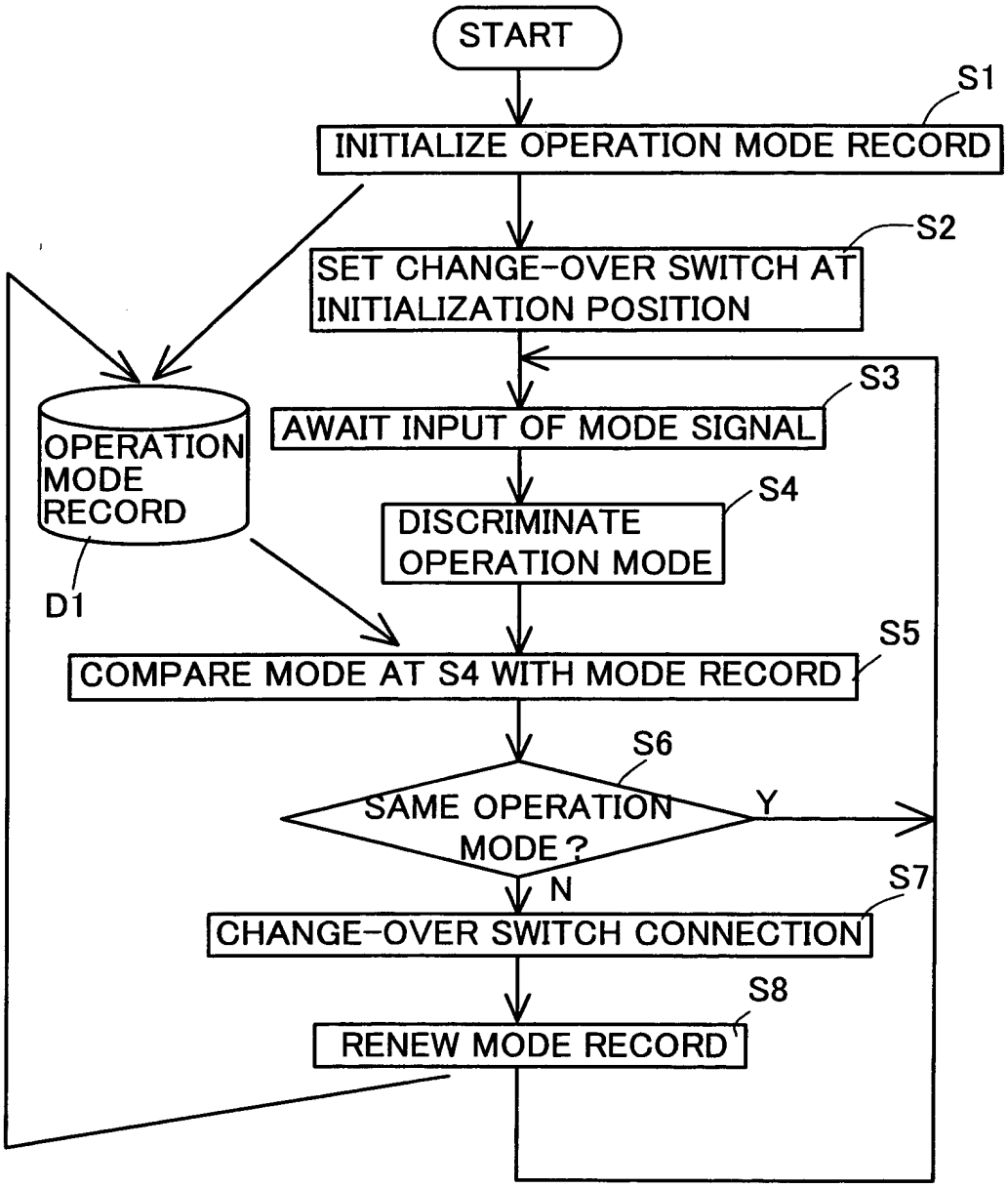

FIG. 4 SEMICONDUCTOR MEMORY DEVICE DIRECTED TO SECOND EMBODIMENT

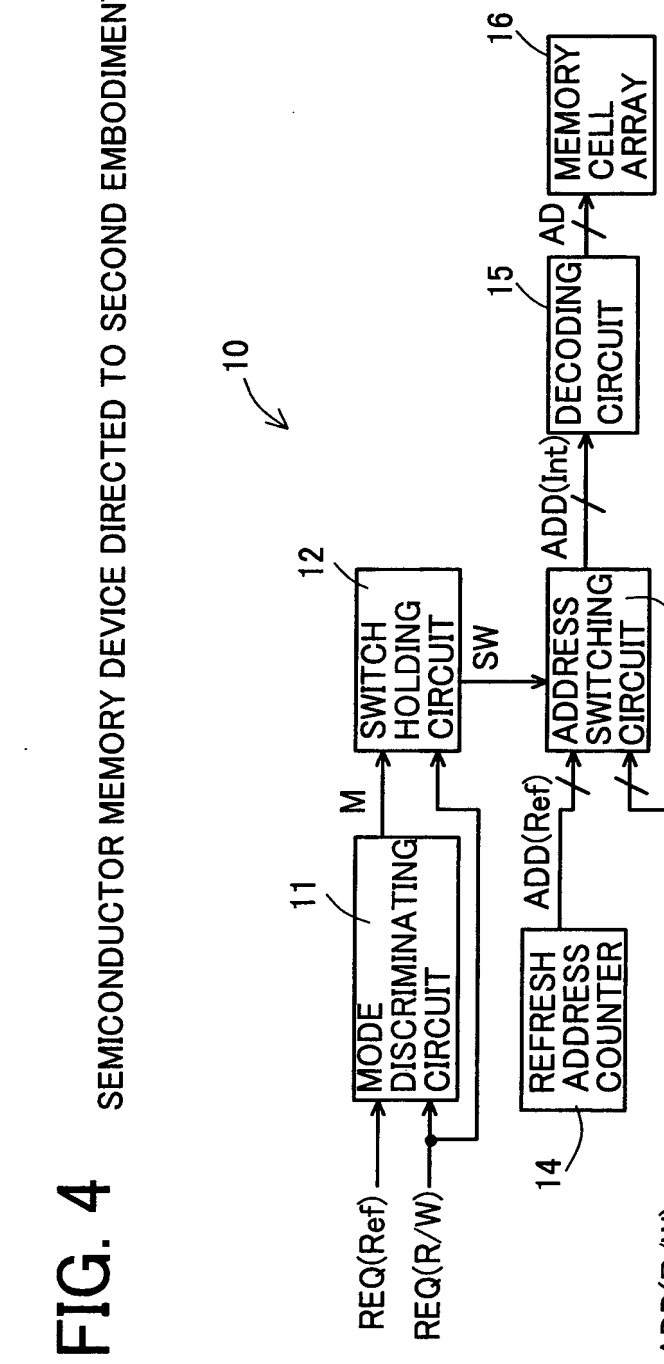

FIG. 5

MODE DISCRIMINATING CIRCUIT

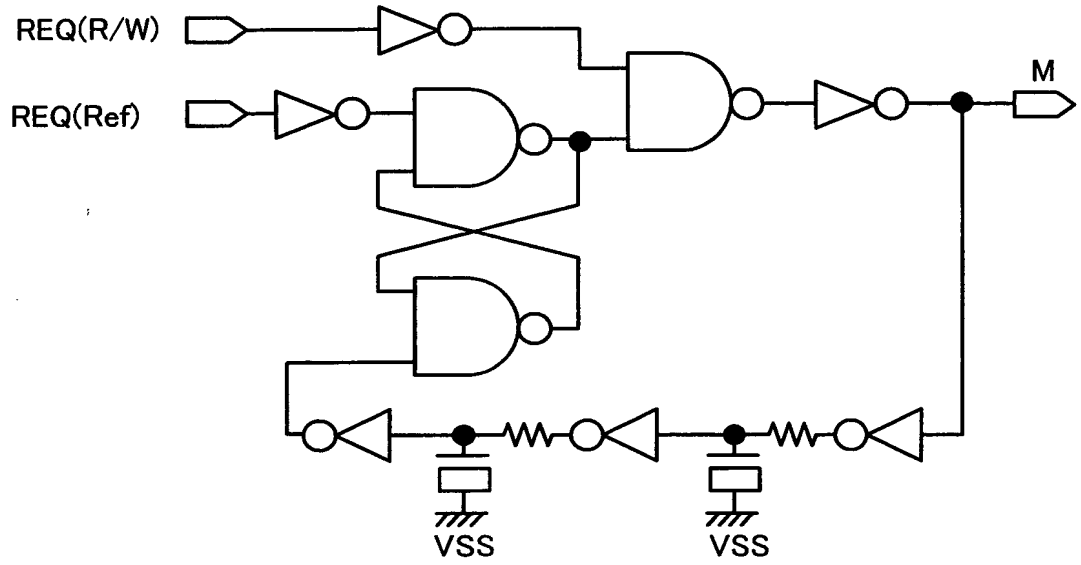

FIG. 6

SWITCH HOLDING CIRCUIT

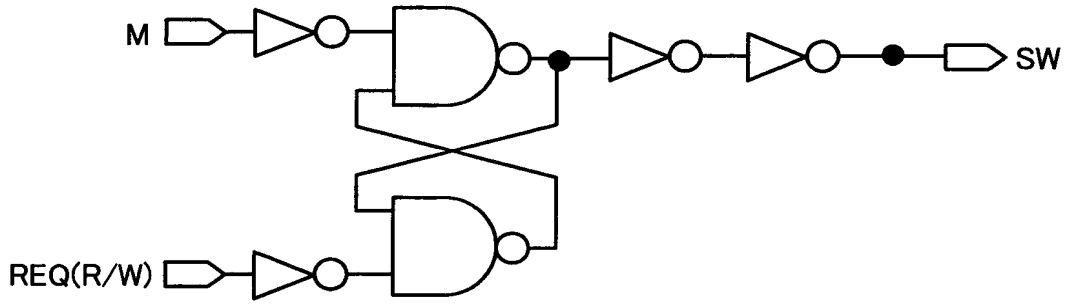

FIG. 7

ADDRESS SWITCHING CIRCUIT

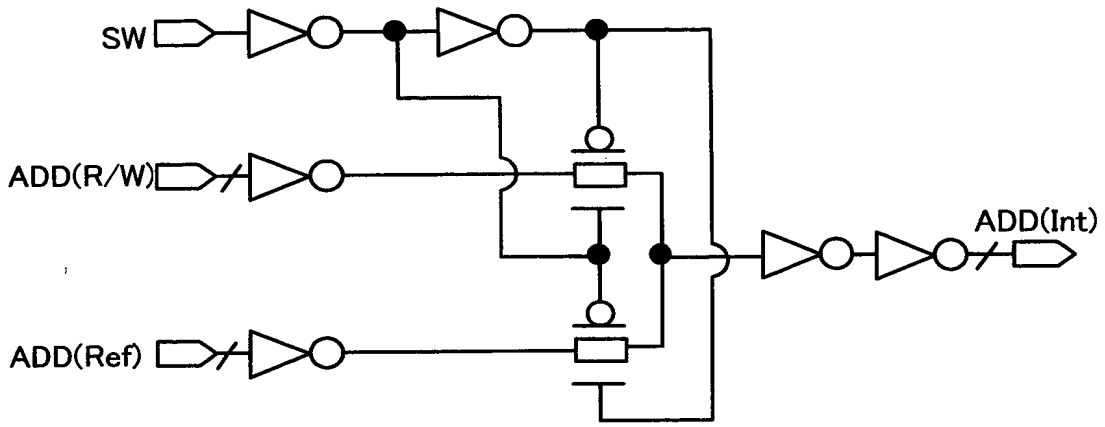

FIG. 8

OPERATIONAL WAVEFORMS DIRECTED TO SECOND EMBODIMENT

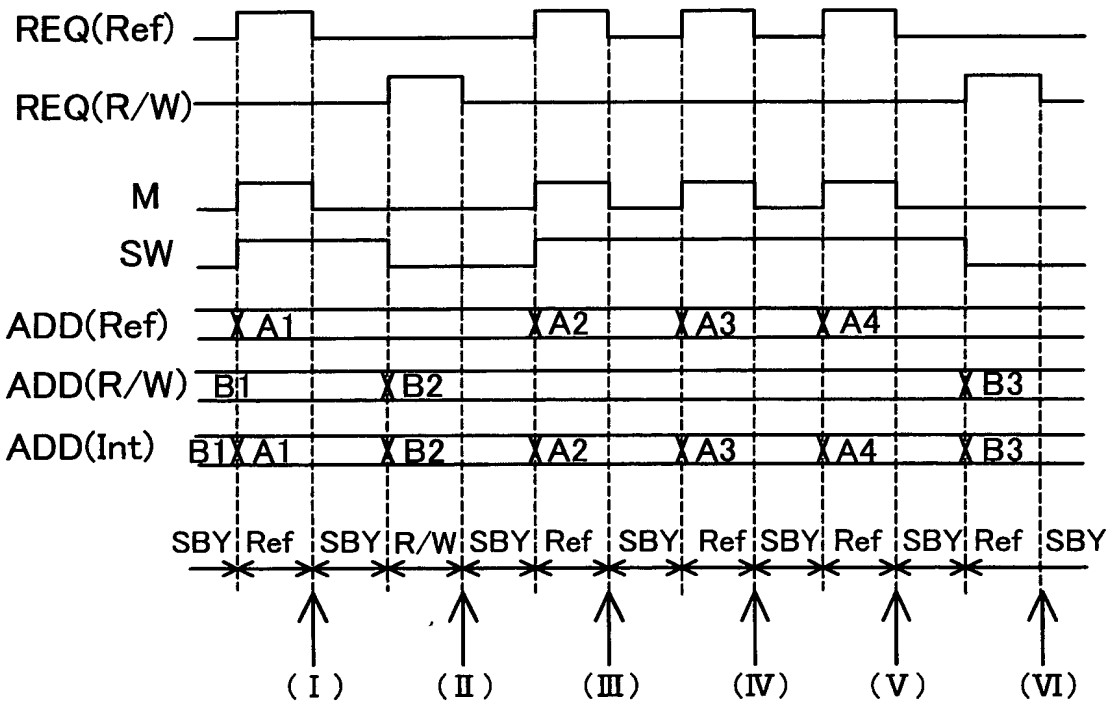

FIG. 9

SYSTEM STRUCTURE FOR REALIZING CONTROL METHOD DIRECTED TO THIRD EMBODIMENT

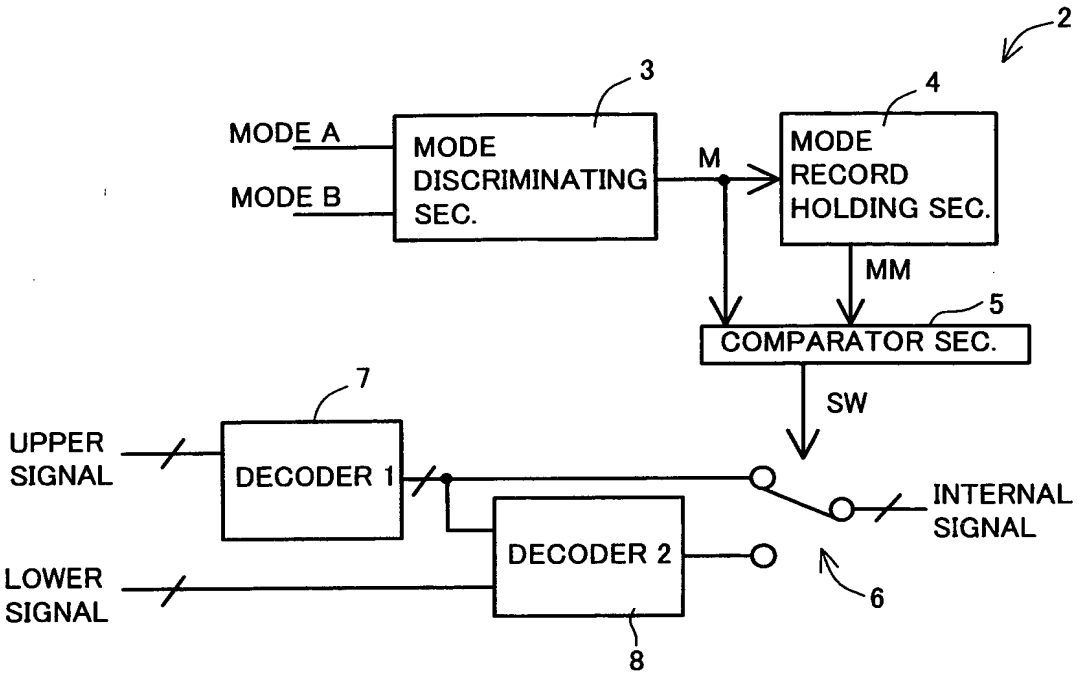

FIG. 10

FLOW CHART SHOWING CONTROL METHOD DIRECTED TO THIRD EMBODIMENT

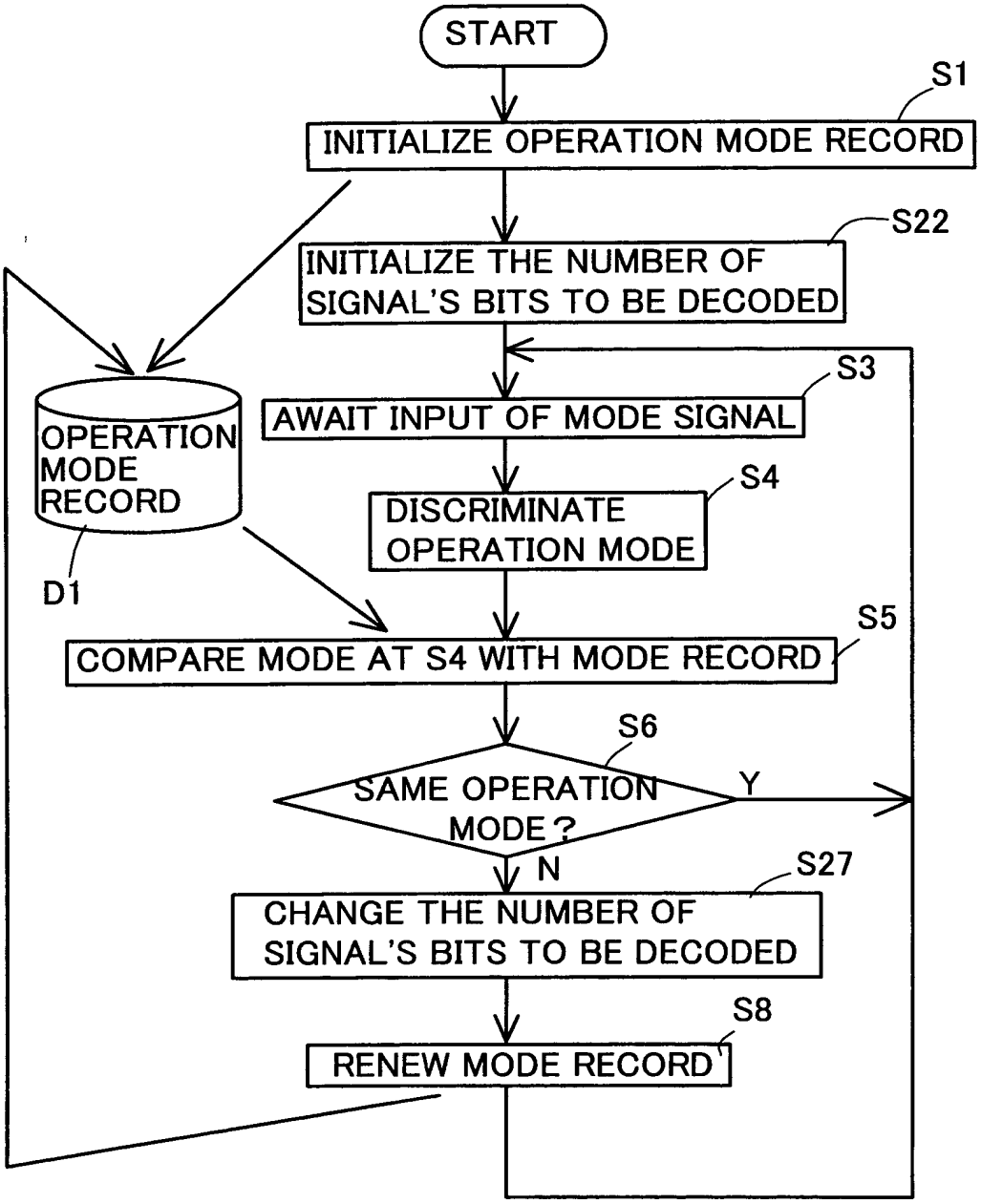

FIG. 11

BLOCK DIAGRAM SHOWING MEMORY ARRAY STRUCTURE OF DRAM

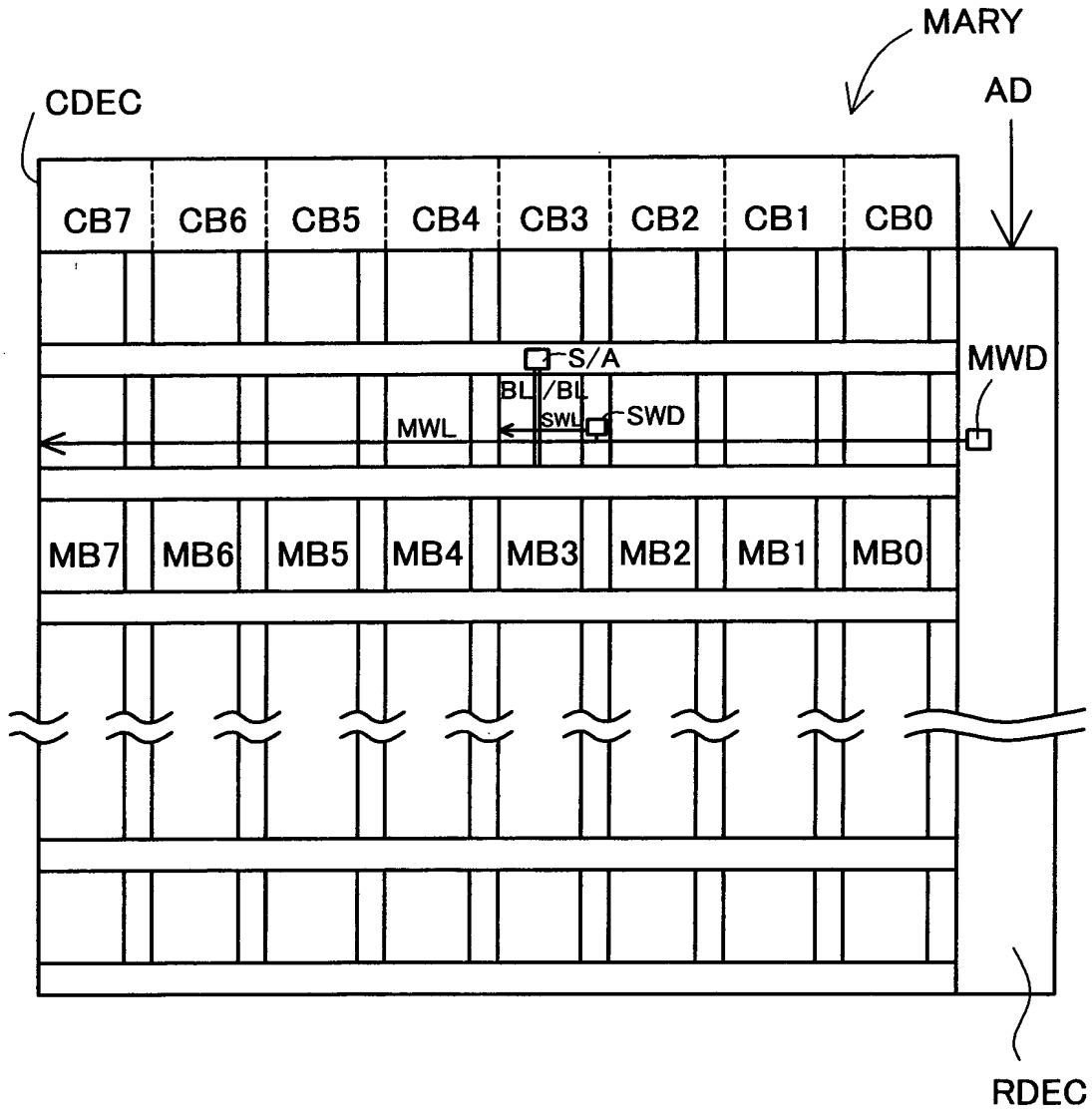

FIG. 12

SEMICONDUCTOR MEMORY DEVICE DIRECTED TO FOURTH EMBODIMENT

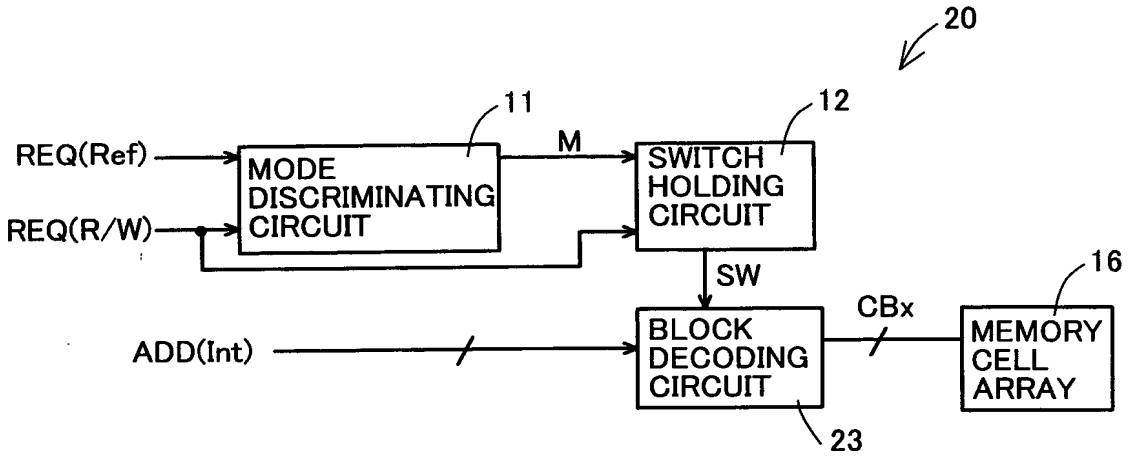

FIG. 13

BLOCK DECODING CIRCUIT

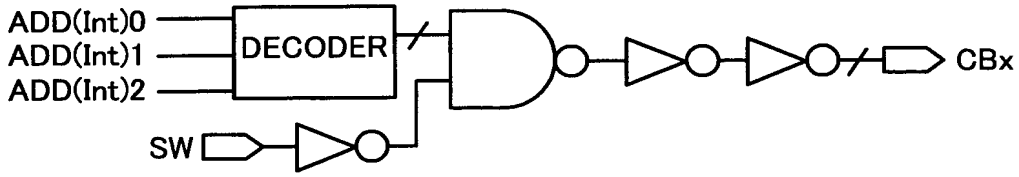

FIG. 14

OPERATIONAL WAVEFORMS DIRECTED TO FOURTH EMBODIMENT

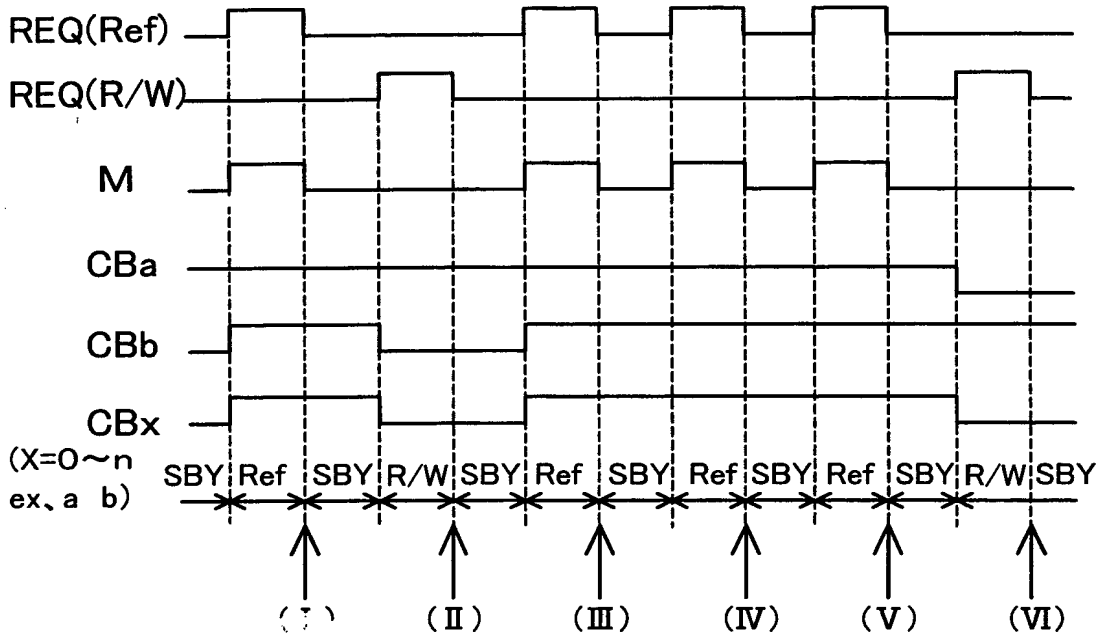

FIG. 15 PRIOR ART

CONVENTIONAL OPERATIONAL WAVEFORMS